LM2775 Switched Capacitor 5-V Boost Converter

1 Features

- 2.7-V to 5.5-V Input Range
- Fixed 5-V Output
- 200-mA Output Current
- Inductorless Solution: Only Requires 3 Small Ceramic Capacitors
- Shutdown Disconnects Load from V_{IN}
- Current Limit and Thermal Protection
- 2-MHz Switching Frequency
- PFM Operation During Light Load Currents (PFM pin tied high)

2 Applications

- USB OTG
- HDMI Power
- Portable Electronics

3 Description

The LM2775 is a regulated switched-capacitor doubler that produces a low-noise output voltage. The LM2775 can supply up to 200 mA of output current over a 3.1-V to 5.5-V input range, as well as up to 125 mA of output current when the input voltage is as low as 2.7 V. At low output currents, the LM2775 can reduce its quiescent current by operating in a pulse frequency modulation (PFM) mode. PFM mode can be enabled or disabled by driving the PFM pin to high or low. Additionally, when the LM2775 is in shutdown, the user can chose to have the output voltage pulled to GND or left in a high impedance state by setting the OUTDIS pin high or low.

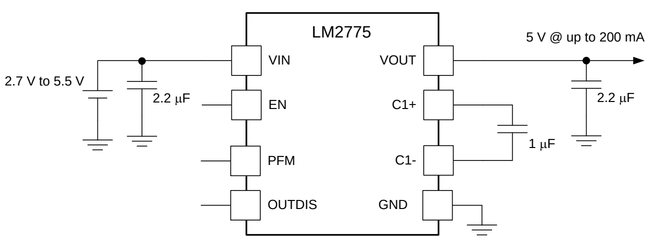
The LM2775 has been placed in TI's 8-pin WSON, a package with excellent thermal properties that keeps the part from overheating under almost all rated operating conditions.

Device Information[(1)]

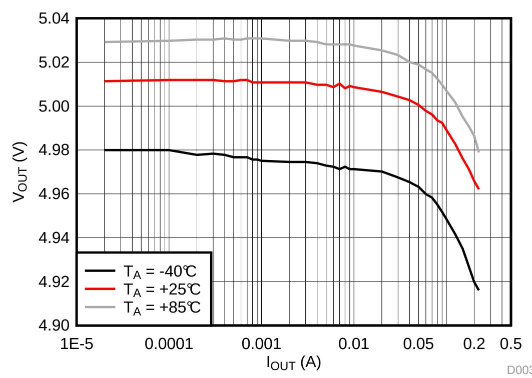
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2775	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



Load Regulation



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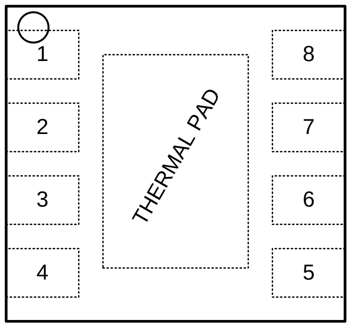
4 Revision History

DATE	REVISION	NOTES
May 2015	*	Initial release.

5 Pin Configuration and Functions

DSG Package
8-Pin WSON with Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PFM	I	PFM mode enable. Allow or disallow PFM operation. 1 = PFM enabled, 0 = PWM disabled
2	C1–	P	Flying capacitor pin
3	C1+	P	Flying capacitor pin
4	OUTDIS	I	Output disconnect option. 1 = Active output discharge during shutdown, 0 = High impedance output without pull-down during shutdown.
5	EN	I	Chip enable. 1 = Enabled, 0 = Disabled
6	VOUT	O	Charge pump output
7	VIN	P	Input voltage
8	GND	G	Ground
Thermal Pad	GND	GND	Connect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
VIN, VOUT	–0.3	6	V
EN, OUTDIS, PFM	–0.3	V_{IN} + 0.3 with 6 V Max	V
Continuous power dissipation	Internally Limited		°C
Junction temperature (T_{J-MAX})		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	2.7		5.5	V
Junction temperature (T_J)	–40		125	°C
Ambient temperature (T_A)	–40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2775 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	41.5	
ψ_{JT}	Junction-to-top characterization parameter	3.2	
ψ_{JB}	Junction-to-board characterization parameter	41.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical limits tested at T_A = 25°C. Minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C). V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 2.2 µF, C1 = 1 µF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage regulation	I_{OUT} = 180 mA	4.8	5	5.2	V
I_Q	Quiescent current	I_{OUT} = 0 mA, PFM = '1'		75	150	µA
		I_{OUT} = 0 mA, PFM = '0'		5		mA
I_{SD}	Shutdown current	EN = '0'		0.7	3	µA
I_{OUTDIS}	Output discharge current	OUTDIS = '1'		500		µA
I_{CL}	Input current limit			600		mA
V_{IL}	Input logic low: EN, OUTDIS, PFM		0		0.4	V
V_{IH}	Input logic high: EN, OUTDIS, PFM		1.2		V_{IN}	V
UVLO	Undervoltage lockout	V_{IN} falling		2.4		V
		V_{IN} rising		2.6		

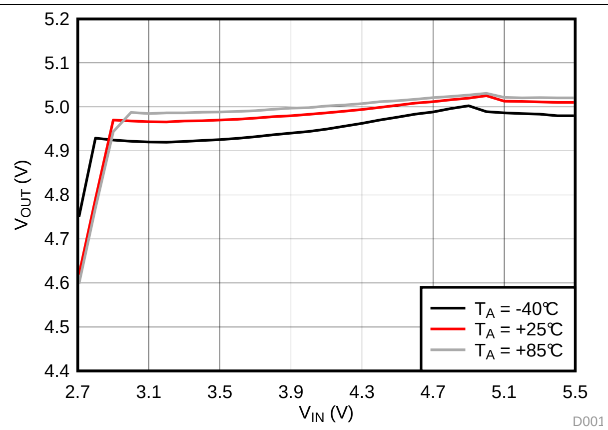
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency		1.7	2	2.3	MHz

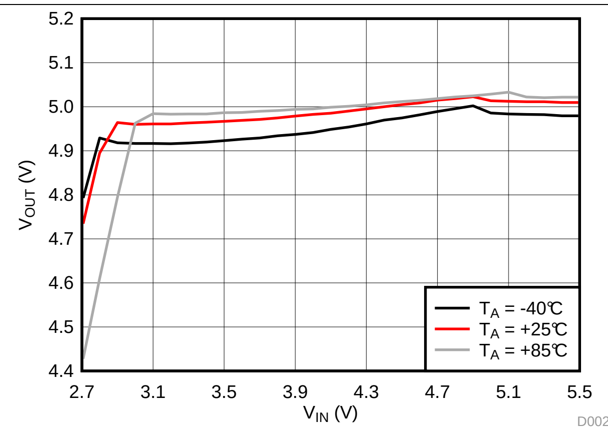
6.7 Typical Characteristics

T_A = 25°C, V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 10 µF (10-V 0402 case), C_1 = 1 µF (10-V 0402 case), V_{EN} = V_{IN}.



I_{LOAD} = 200 mA PFM = '0'

Figure 1. PWM Output Regulation

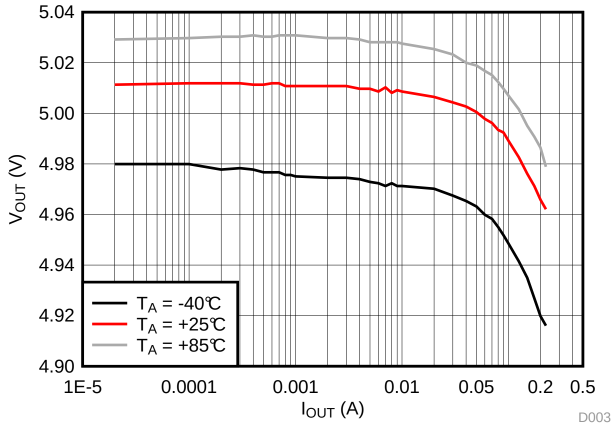


I_{LOAD} = 200 mA PFM = '1'

Figure 2. PFM Output Regulation

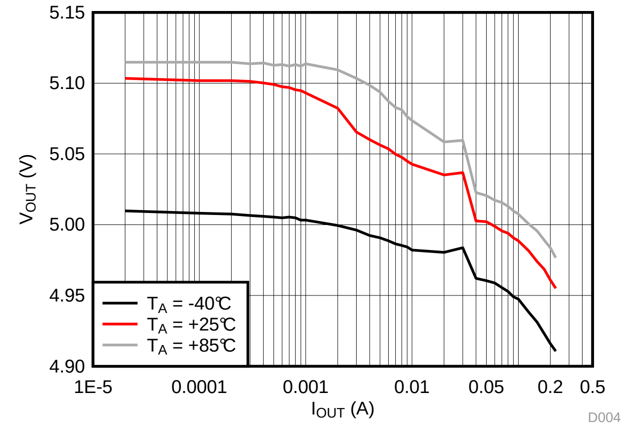
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 10 µF (10-V 0402 case), C_1 = 1 µF (10-V 0402 case), V_{EN} = V_{IN}.



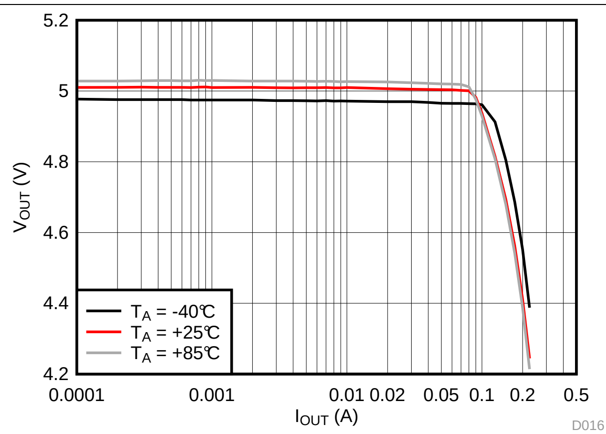
V_{IN} = 3.3 V PFM = '0'

Figure 3. Load Regulation



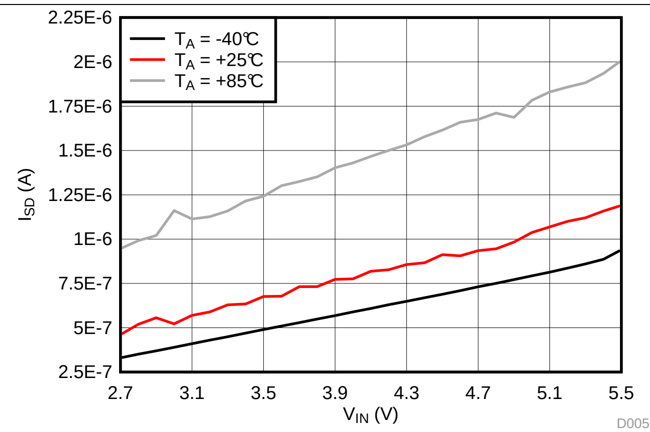
V_{IN} = 3.3 V PFM = '1'

Figure 4. Load Regulation



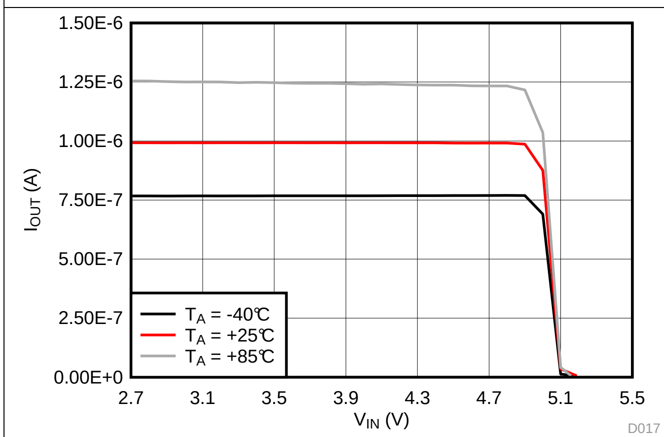
V_{IN} = 2.7 V PFM = '0'

Figure 5. Load Regulation



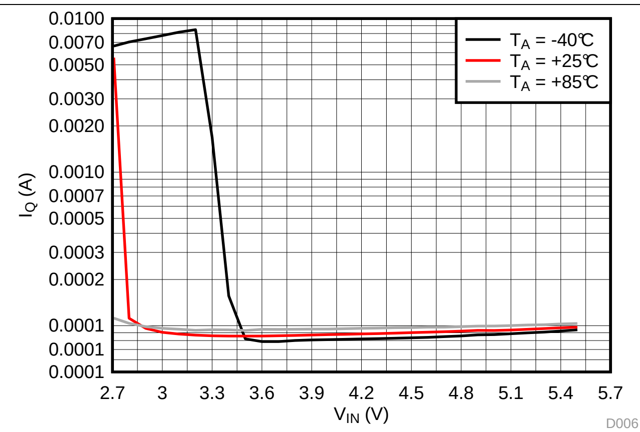
EN = '0'

Figure 6. Shutdown Current



EN = '0' OUTDIS = '0'

Figure 7. Output Leakage Current

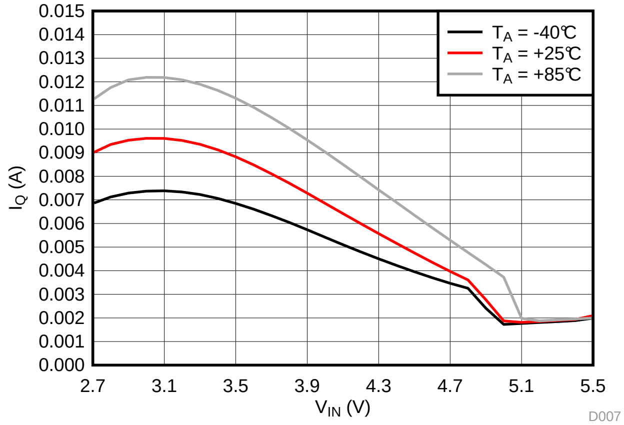


I_{LOAD} = 0 mA PFM = '1'

Figure 8. PFM Quiescent Current

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 10 µF (10-V 0402 case), C_1 = 1 µF (10-V 0402 case), V_{EN} = V_{IN}.



I_{LOAD} = 0 mA PFM = '0'

Figure 9. PWM Quiescent Current

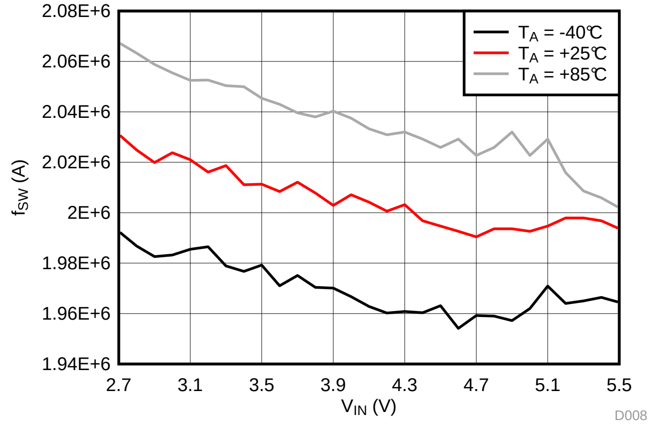
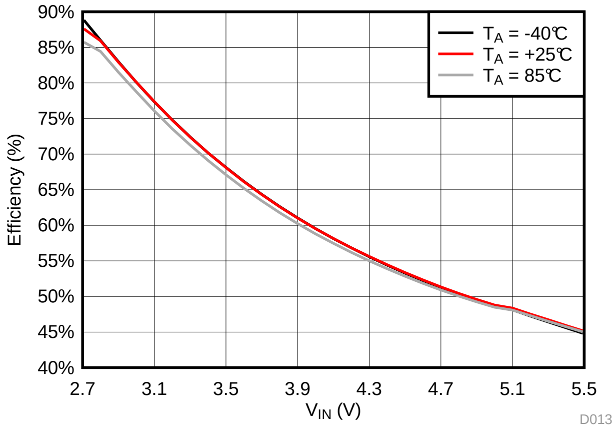
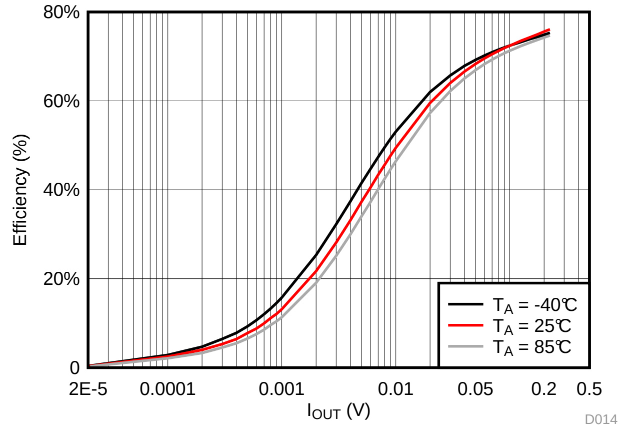


Figure 10. Switching Frequency



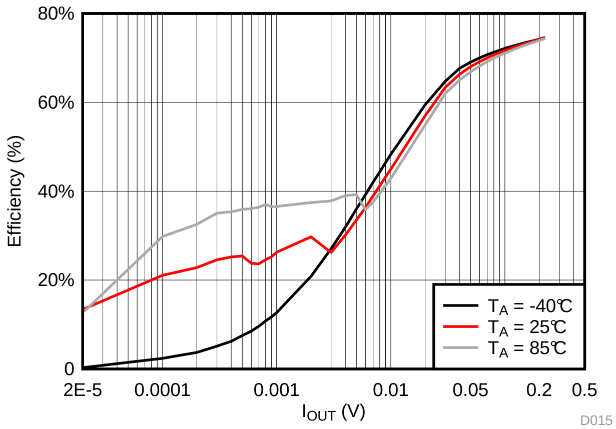
I_{LOAD} = 100 mA PFM = '0'

Figure 11. Efficiency vs Input Voltage



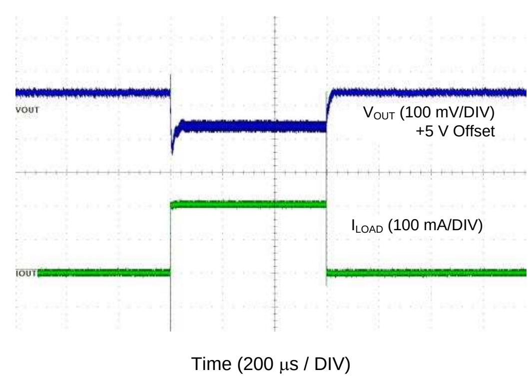
V_{IN} = 3.3 V PFM = '0'

Figure 12. Efficiency vs Load Current



V_{IN} = 3.3 V PFM = '1'

Figure 13. Efficiency vs Load Current

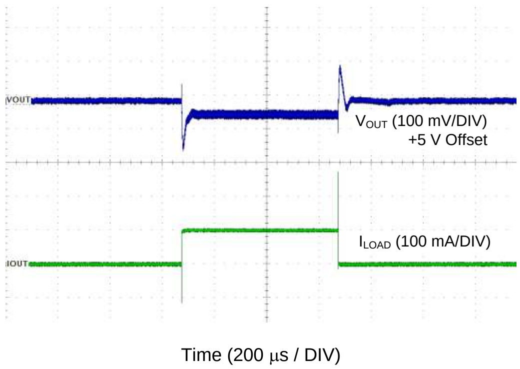


V_{IN} = 3.6 V I_{LOAD} = 1 mA to 100 mA PFM = '1'

Figure 14. PFM Load Step

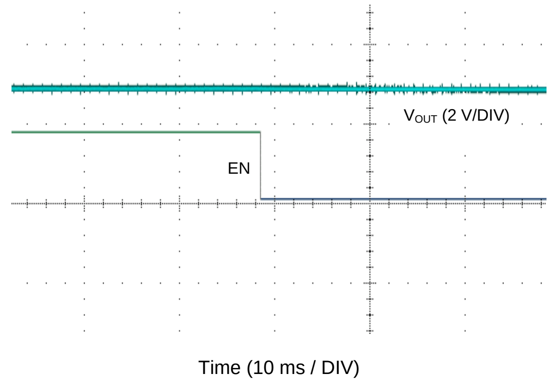
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 3.6 V, C_{IN} = C_{OUT} = 10 µF (10-V 0402 case), C_1 = 1 µF (10-V 0402 case), V_{EN} = V_{IN}.



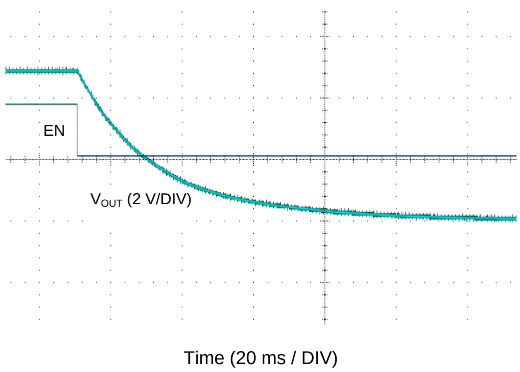
V_{IN} = 3.6 V I_{LOAD} = 1 mA to 100 mA PFM = '0'

Figure 15. PWM Load Step



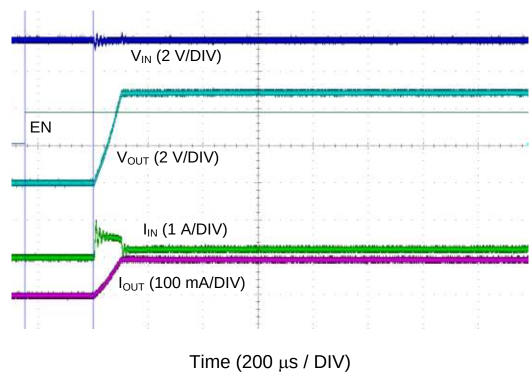
V_{IN} = 3.6 V OUTDIS = '0'

Figure 16. Output Discharge Disabled



V_{IN} = 3.6 V OUTDIS = '1'

Figure 17. Output Discharge Enabled



V_{IN} = 3.6 V I_{LOAD} = 100 mA

Figure 18. Start-Up into a Load

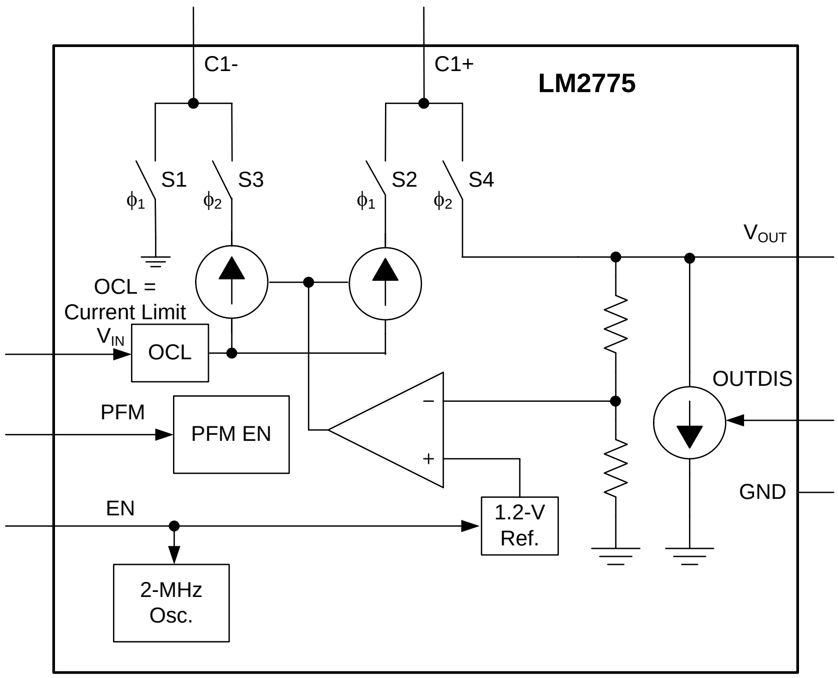
7 Detailed Description

7.1 Overview

The LM2775 is a regulated switched capacitor doubler that, by combining the principles of switched-capacitor voltage boost and linear regulation, generates a regulated output from an extended Li-Ion input voltage range. A two-phase non-overlapping clock generated internally controls the operation of the doubler. During the charge phase (φ1), the flying capacitor (C1) is connected between the input and ground through internal pass transistor switches and is charged to the input voltage. In the pump phase that follows (φ2), the flying capacitor is connected between the input and output through similar switches. Stacked atop the input, the charge of the flying capacitor boosts the output voltage and supplies the load current.

A traditional switched capacitor doubler operating in this manner uses switches with very low on-resistance to generate an output voltage that is 2× the input voltage. Regulation is achieved by modulating the current of the two switches connected to the VIN pin (one switch in each phase).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pre-Regulation

The very low input current ripple of the LM2775, resulting from internal pre-regulation, adds minimal noise to the input line. The core of the LM2775 is very similar to that of a basic switched capacitor doubler: it is composed of four switches and a flying capacitor (external). Regulation is achieved by controlling the current through the two switches connected to the VIN pin (one switch in each phase). The regulation is done before the voltage doubling, giving rise to the term "pre-regulation". It is pre-regulation that eliminates most of the input current ripple that is a typical and undesirable characteristic of a many switched capacitor converters.

7.3.2 Input Current Limit

The LM2775 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The input current is limited to 600 mA (typical) when the output is shorted directly to ground. When the LM2775 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling should be expected.

Feature Description (continued)

7.3.3 PFM Mode

To minimize quiescent current during light load operation, the LM2775 provides a PFM operation option (selectable via the PFM pin. '1' = PFM allowed, '0' = Fixed frequency). By allowing the charge pump to only switch when the V_{OUT} voltage decays to a typical 5.05 V, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-1-kHz range when unloaded. As the load increases, the frequency of pulsing increases.

When PFM mode is disabled, the device operates in a constant frequency mode. In this mode, the quiescent current remains at normal levels even when the load current is decreased. The main advantages of fixed frequency operation include a lower output voltage ripple level due to the constant switching and a predictable switching frequency that stays at 2 MHz which can be important in noise sensitive applications.

7.3.4 Output Discharge

The LM2775 provides two different output discharge modes upon entering a shutdown state (EN pin = '0') after running in the on state (EN = '1'). The first mode is high impendance mode (OUTDIS = '0'). In this mode, the output remains high even when the EN pin is driven low. This enables use in applications where the LM2775 output might be tied to a system rail that has another power source connected (USBOTG). When OUTDIS = 0, the output of the LM2775 draws a minimal current from the output supply (1.6 µA typical).

In Discharge Mode (OUTDIS pin = '1'), the LM2775 actively pulls down on the output of the device until the output voltage reaches GND. In this mode, the current drawn from the output is approximately 450 µA.

7.3.5 Thermal Shutdown

The LM2775 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the part switches into shutdown mode. The LM2775 releases thermal shutdown when the junction temperature of the part is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. LM2775 power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped be reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the LM2775. The WSON package is designed to have excellent thermal properties that, when soldered to a PCB designed to aid thermal dissipation, allows the LM2775 to operate under very demanding power dissipation conditions.

7.3.6 Undervoltage Lockout

The LM2775 has an internal comparator that monitors the voltage at VIN and forces the LM2775 into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM2775 resumes normal operation

7.4 Device Functional Modes

7.4.1 Shutdown

The LM2775 enters Shutdown Mode if one of the two conditions are met.

- If V_{IN} is removed or allowed to sag to ground, the device enters shutdown.
- If the EN pin is driven low when V_{IN} is within the normal operating range.

In Shutdown, the LM2775 typically draws less than 1 µA from the supply. Depending on the state of the OUTDIS pin, the output is pulled low when entering shutdown (OUTDIS = '1'), or it remains near the final output voltage with the output in a low leakage state (OUTDIS = '0').

7.4.2 Boost Mode

The LM2775 is in Boost Mode if V_{IN} is within the normal operating range, and the EN pin is driven high. Depending on the state of the PFM pin, the LM2775 either regulates the output via a PFM burst mode (PFM = '1') or via a constant switching mode (PFM = '0').

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2775 can create a 5-V system rail capable of delivering up to 200 mA of output current to the load. The 2-MHz switched capacitor boost allows for the use of small value discrete external components.

8.2 Typical Application

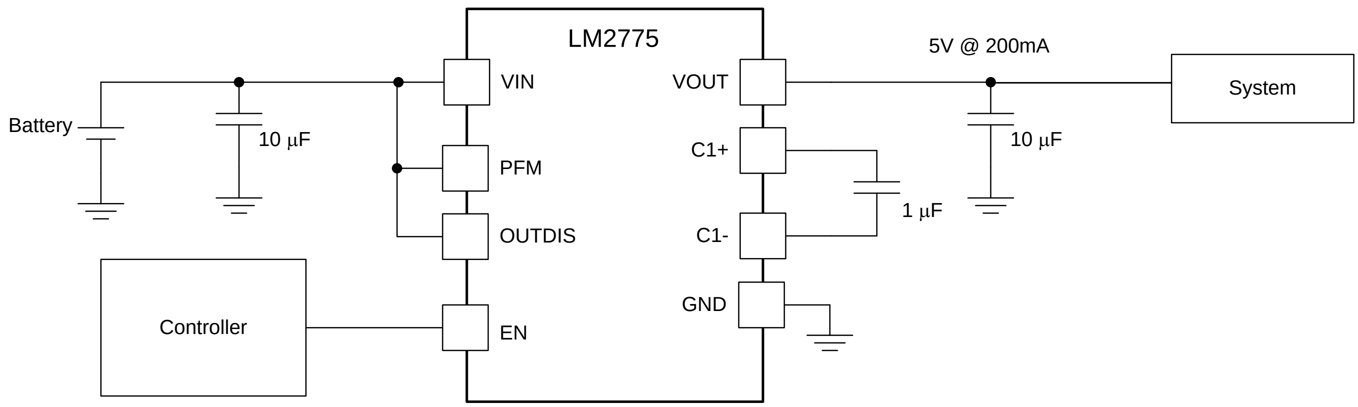


Figure 19. Typical LM2775 Configuration

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Output current range	0 mA to 200 mA (Max. current will depend on V_{IN})

8.2.2 Detailed Design Procedure

8.2.2.1 Output Current Capability

The LM2775 provides 200 mA of output current when the input voltage is within 3.1 V to 5.5 V.

NOTE

Understanding relevant application issues is recommended and a thorough analysis of the application circuit should be performed when using the part outside operating ratings and/or specifications to ensure satisfactory circuit performance in the application. Special care should be paid to power dissipation and thermal effects. These parameters can have a dramatic impact on high-current applications, especially when the input voltage is high. (see the *Power Dissipation* section).

The schematic of Figure 20 is a simplified model of the LM2775 that is useful for evaluating output current capability. The model shows a linear pre-regulation block (Reg), a voltage doubler (2×), and an output resistance (R_{OUT}). Output resistance models the output voltage droop that is inherent to switched capacitor converters. The output resistance of the LM2775 is 3.5 Ω (typical) and is approximately equal to twice the resistance of the four LM2775 switches. When the output voltage is in regulation, the regulator in the model controls the voltage V' to keep the output voltage equal to 5 V ± 4%. With increased output current, the voltage drop across R_{OUT}

increases. To prevent droop in output voltage, the voltage drop across the regulator is reduced, V' increases, and V_{OUT} remains at 5 V. When the output current increases to the point that there is zero voltage drop across the regulator, V' equals the input voltage, and the output voltage is near the edge of regulation. Additional output current causes the output voltage to fall out of regulation, and the LM2775 operation is similar to a basic open-loop doubler. As in a voltage doubler, increase in output current results in output voltage drop proportional to the output resistance of the doubler. The out-of-regulation LM2775 output voltage can be approximated by:

$$V_{OUT} = 2 \times V_{IN} - I_{OUT} \times R_{OUT} \quad (1)$$

Again, Equation 1 only applies at low input voltage and high output current where the LM2775 is not regulating. See *Output Current vs. Output Voltage* curves in the *Typical Characteristics* section for more details.

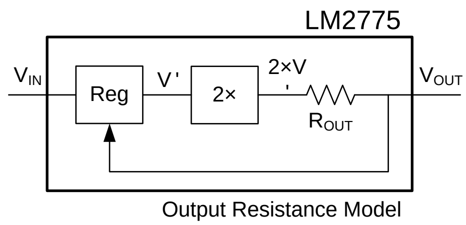


Figure 20. LM2775 Output Resistance Model

A more complete calculation of output resistance takes into account the effects of switching frequency, flying capacitance, and capacitor equivalent series resistance (ESR) (see Equation 2).

$$R_{OUT} = 2 \cdot R_{SW} + \frac{1}{F_{SW} \times C_1} + 4 \cdot ESR_{C1} + ESR_{COUT} \quad (2)$$

Switch resistance component (3 Ω typical) dominates the output resistance equation of the LM2775. With a 2-MHz typical switching frequency, the 1/(F×C) component of the output resistance contributes only 0.5 Ω to the total output resistance. Increasing the flying capacitance only provides minimal improvement to the total output current capability of the LM2775. In some applications it may be desirable to reduce the value of the flying capacitor below 1 µF to reduce solution size and/or cost, but this should be done with care so that output resistance does not increase to the point that undesired output voltage droop results. If ceramic capacitors are used, ESR will be a negligible factor in the total output resistance, as the ESR of quality ceramic capacitors is typically much less than 100 mΩ.

8.2.2.2 Efficiency

Charge-pump efficiency is derived in Equation 3 and Equation 4 (supply current and other losses are neglected for simplicity):

$$I_{IN} = G \times I_{OUT} \; E = (V_{OUT} \times I_{OUT}) \div (V_{IN} \times I_{IN}) = V_{OUT} \div (G \times V_{IN}) \quad (3)$$

If one includes the quiescent current drawn by the LM2775 to operate, the following can be derived :

$$E = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (2 \cdot I_{OUT} + I_Q)} \quad (4)$$

In Equation 3, G represents the charge pump gain. Efficiency is at its highest as G × V_{IN} approaches V_{OUT}. For the LM2775 device, G = 2.

8.2.2.3 Power Dissipation

LM2775 power dissipation (P_D) is calculated simply by subtracting output power from input power:

$$P_D = P_{IN} - P_{OUT} = [V_{IN} \times (2 \times I_{OUT} + I_Q)] - [V_{OUT} \times I_{OUT}] \quad (5)$$

Power dissipation increases with increased input voltage and output current, up to 1.35 W at the ends of the operating ratings (V_{IN} = 5.5 V, I_{OUT} = 200 mA). Internal power dissipation self-heats the device. Dissipating this amount power/heat so the LM2775 does not overheat is a demanding thermal requirement for a small surface-mount package. When soldered to a PCB with layout conducive to power dissipation, the excellent thermal properties of the WSON package enable this power to be dissipated from the LM2775 with little or no derating, even when the circuit is placed in elevated ambient temperatures.

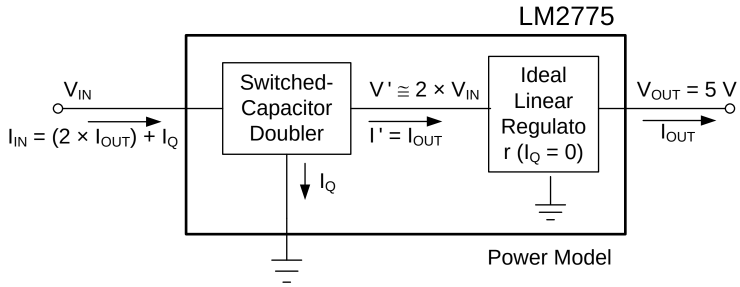


Figure 21. Power Model

8.2.2.4 Recommended Capacitor Types

The LM2775 requires 3 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low ESR (≤ 15 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM2775 due to their high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferred for use with the LM2775. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over –55°C to 125°C; X5R: ±15% over –55°C to 85°C).

Capacitors with a Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2775. These types of capacitors typically have wide capacitance tolerance (80% to 20%) and vary significantly over temperature (Y5V: 22%, –82% over –30°C to 85°C range; Z5U: 22%, –56% over 10°C to 85°C range). Under some conditions, a 1-µF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2775.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower capacitance than expected on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC-bias voltages significantly below the capacitor voltage rating usually minimizes DC-bias effects. Consult capacitor manufacturers for information on capacitor DC-bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. It is strongly recommended that the LM2775 circuit be thoroughly evaluated early in the design-in process with the mass-production capacitors of choice. This helps ensure that any such variability in capacitance does not negatively impact circuit performance.

The voltage rating of the output capacitor should be 10 V or more. All other capacitors should have a voltage rating at or above the maximum input voltage of the application.

8.2.2.5 Output Capacitor and Output Voltage Ripple

The output capacitor in the LM2775 circuit (C_{OUT}) directly impacts the magnitude of output voltage ripple. Other prominent factors also affecting output voltage ripple include input voltage, output current, and flying capacitance. One important generalization can be made: increasing (decreasing) the output capacitance results in a proportional decrease (increase) in output voltage ripple. A simple approximation of output ripple is determined by calculating the amount of voltage droop that occurs when the output of the LM2775 is not being driven. This occurs during the charge phase (φ1). During this time, the load is driven solely by the charge on the output capacitor. The magnitude of the ripple thus follows the basic discharge equation for a capacitor (I = C × dV/dt), where discharge time is one-half the switching period, or $0.5/F_{SW}$ (see Equation 6).

$$\text{RIPPLE}_{\text{Peak-Peak}} = \frac{I_{OUT}}{C_{OUT}} \times \frac{0.5}{F_{SW}} \tag{6}$$

A more thorough and accurate examination of factors that affect ripple requires including effects of phase non-overlap times and output capacitor ESR. In order for the LM2775 to operate properly, the two phases of operation must never coincide. (If this were to happen all switches would be closed simultaneously, shorting input, output, and ground). Thus, non-overlap time is built into the clocks that control the phases. Since the output is not being driven during the non-overlap time, this time should be accounted for in calculating ripple. Actual output capacitor discharge time is approximately 60% of a switching period, or $0.6/F_{SW}$ (see Equation 7).

$$RIPPLE_{Peak-Peak} = \left(\frac{I_{OUT}}{C_{OUT}} \times \frac{0.6}{F_{SW}} \right) + \left(2 \times I_{OUT} \times ESR_{COUT} \right) \tag{7}$$

NOTE

In typical high-current applications, a 10-µF, 10-V low-ESR ceramic output capacitor is recommended. Different output capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the output capacitor may also require changing the flying capacitor and/or input capacitor to maintain good overall circuit performance. If a small output capacitor is used and PFM mode is enabled, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2-µF capacitance is recommended. For example, a 10-µF, 10-V output capacitor in a 0402 case size will typically only have 2-µF capacitance when biased to 5 V.

High ESR in the output capacitor increases output voltage ripple. If a ceramic capacitor is used at the output, this is usually not a concern because the ESR of a ceramic capacitor is typically very low and has only a minimal impact on ripple magnitudes. If a different capacitor type with higher ESR is used (tantalum, for example), the ESR could result in high ripple. To eliminate this effect, the net output ESR can be significantly reduced by placing a low-ESR ceramic capacitor in parallel with the primary output capacitor. The low ESR of the ceramic capacitor is in parallel with the higher ESR, resulting in a low net ESR based on the principles of parallel resistance reduction.

8.2.2.6 Input Capacitor and Input Voltage Ripple

The input capacitor (C_{IN}) is a reservoir of charge that aids a quick transfer of charge from the supply to the flying capacitor during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitor is connected to the input. It also filters noise on the input pin, keeping this noise out of sensitive internal analog circuitry that is biased off the input line.

Much like the relationship between the output capacitance and output voltage ripple, input capacitance has a dominant and first-order effect on input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affect input ripple levels to some degree.

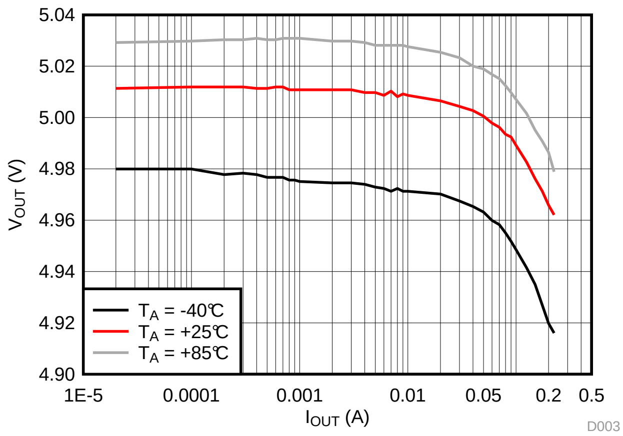
In typical high-current applications, a 10-µF low-ESR ceramic capacitor is recommended on the input. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution. But changing the input capacitor may also require changing the flying capacitor and/or output capacitor to maintain good overall circuit performance.

8.2.2.7 Flying Capacitor

The flying capacitor (C1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM2775 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 1-µF low-ESR ceramic capacitors are recommended for the flying capacitor. Polarized capacitors (tantalum, aluminum electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM2775 operation.

8.2.3 Application Curve



V_{IN} = 3.3 V PFM = '0'

Figure 22. Load Regulation

8.2.4 USB OTG / Mobile HDMI Power Supply

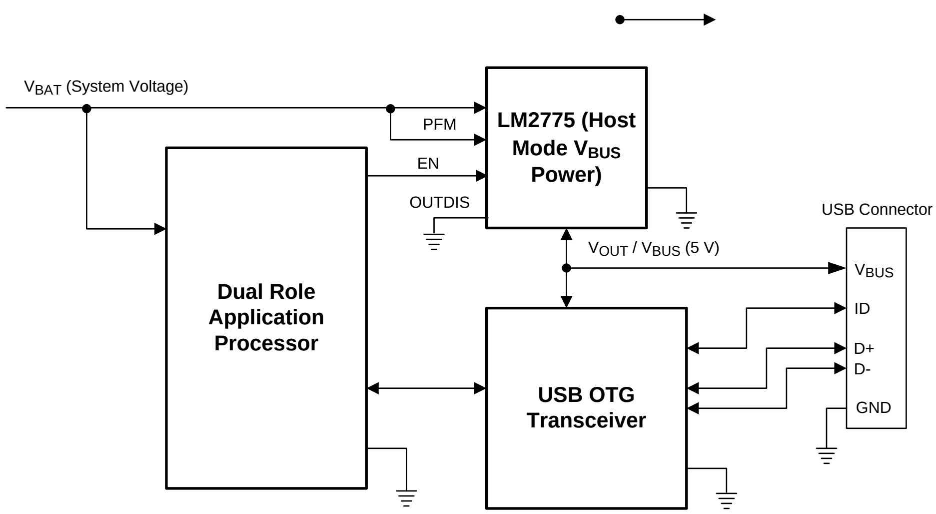


Figure 23. USB OTG Configuration

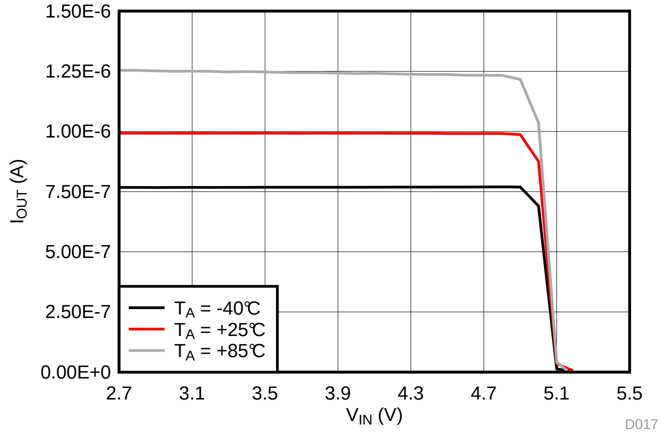
8.2.4.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 5.5 V
Output current range	0 mA to 200 mA (Max. current will depend on V_{IN})

8.2.4.2 Detailed Design Procedure

The 5-V output mode is normally used for the USB OTG / Mobile HDMI application. Therefore, the LM2775 can be enabled/disabled by applying a logic signal on only the EN pin while grounding the OUTDIS pin. Depending on the USB/HDMI mode of the application, the LM2775 can be enabled to drive the power bus line (Host), or disabled to put its output in high impedance allowing an external supply to drive the bus line (Slave). In addition to the high impedance-backdrive protection, the output current limit protection is 250 mA (typical), well within the USB OTG and HDMI requirements.

8.2.4.3 Application Curve



EN = '0' OUTDIS = '0'

Figure 24. Output Leakage Current High Z

9 Power Supply Recommendations

The LM2775 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2775 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

Proper board layout helps to ensure optimal performance of the LM2775 circuit. The following guidelines are recommended:

- Place capacitors as close to the LM2775 as possible, and preferably on the same side of the board as the device.
- Use short, wide traces to connect the external capacitors to the LM2775 to minimize trace resistance and inductance.
- Use a low resistance connection between ground and the GND pin of the LM2775. Using wide traces and/or multiple vias to connect GND to a ground plane on the board is most advantageous.

10.2 Layout Example

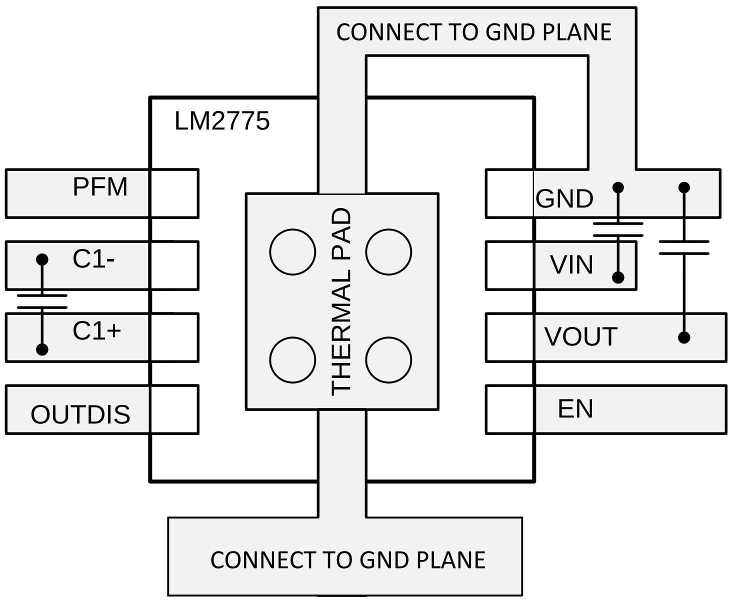


Figure 25. Example LM2775 Layout

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2775DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2775	Samples
LM2775DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2775	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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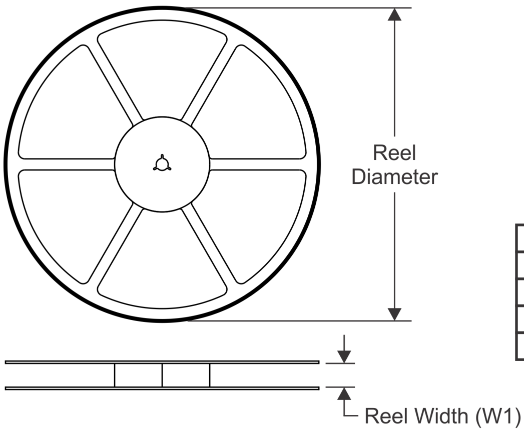
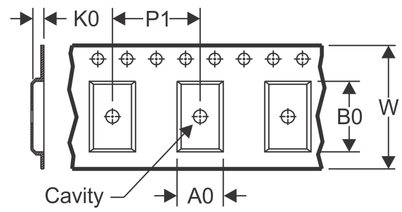
TAPE AND REEL INFORMATION

REEL DIMENSIONS

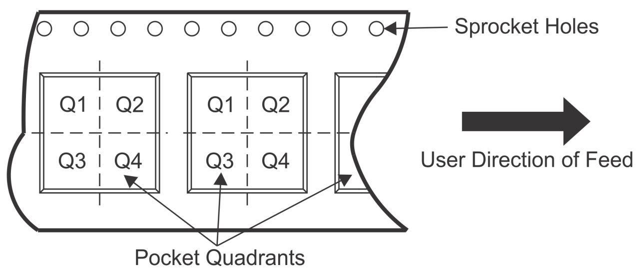


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

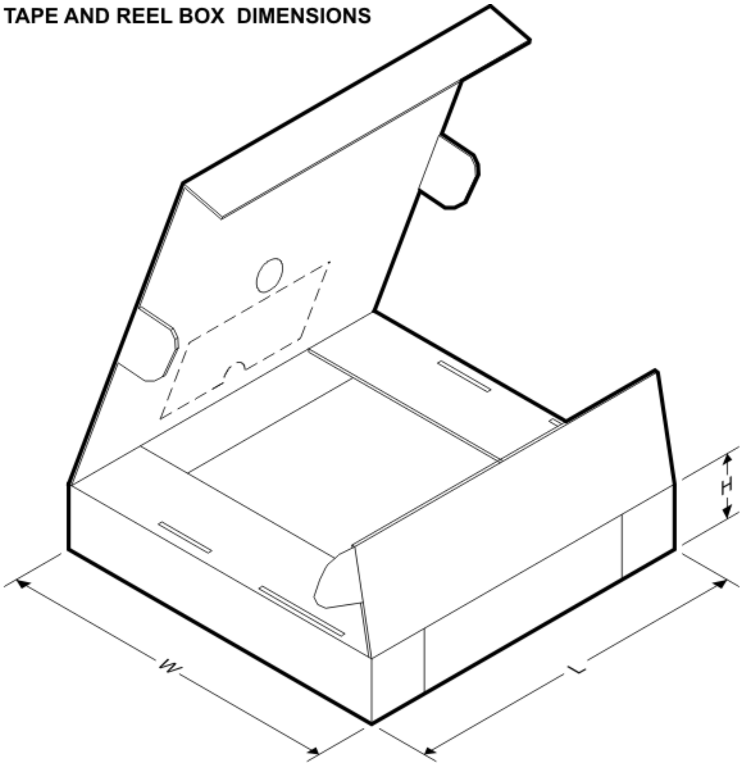
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2775DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM2775DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

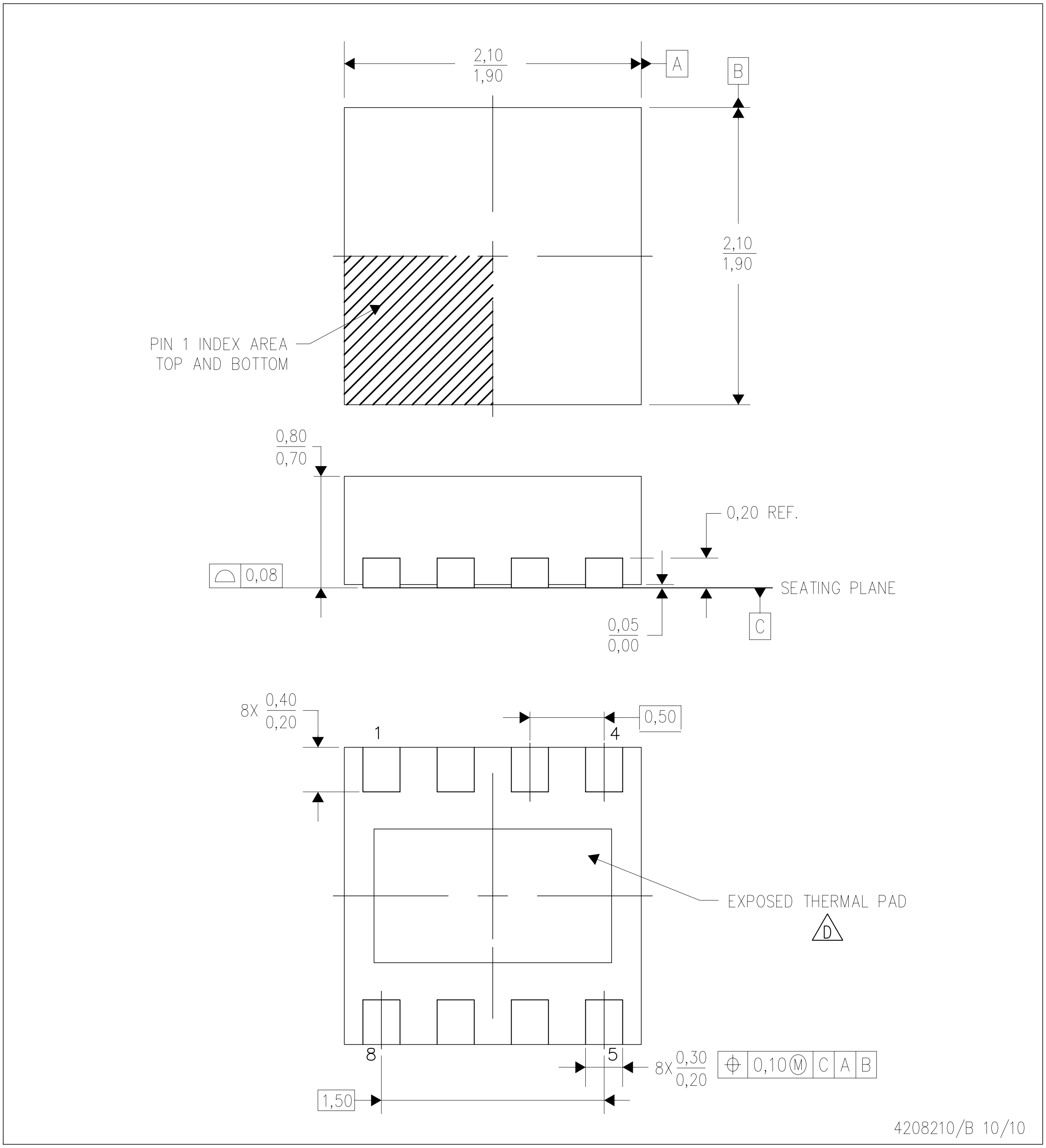
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2775DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM2775DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–229.

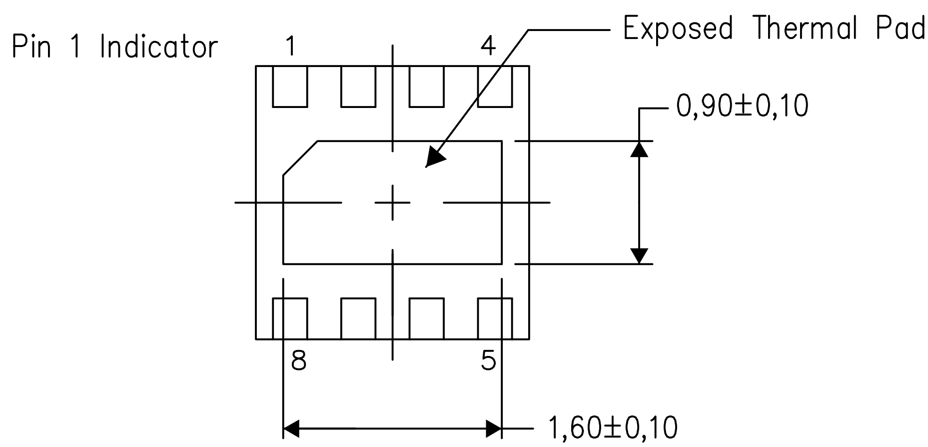
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



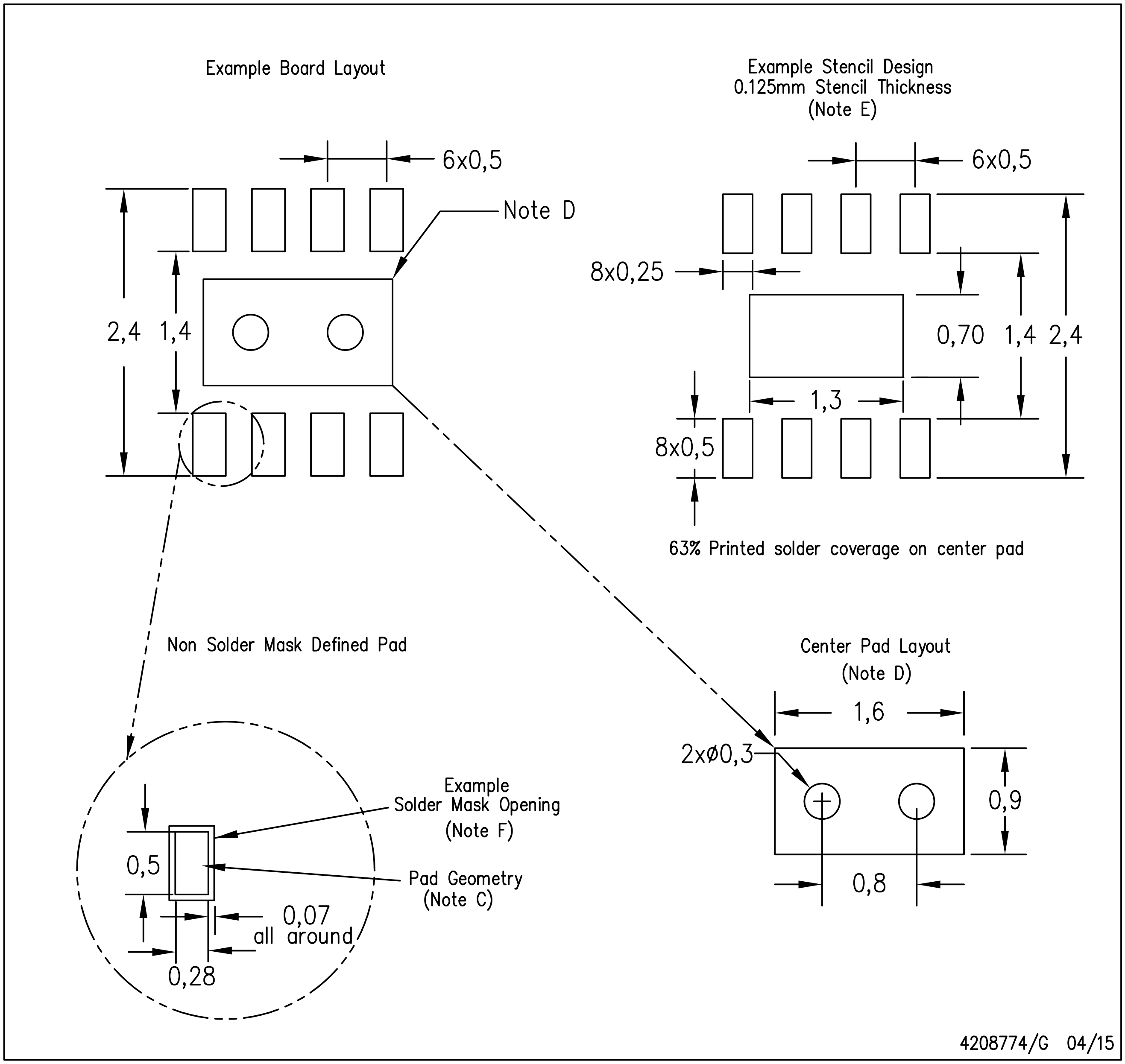
Bottom View

Exposed Thermal Pad Dimensions

4208347/H 04/15

NOTE: All linear dimensions are in millimeters

DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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